

# Extendibility of Cu/low-k/airgap BEOL

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Coverage of IBM’s Cu ULSI interconnect technologies will be presented, from the first introduction to the present day, and extending to the future with scaling and novel enhancements. This topic (BEOL, back end of line) has undergone a long revolution over the past 10 years, as it has risen from less-important stature in integrated circuits to among the forefront efforts in modern materials and integration engineering. As well, its introduction and adoption by the industry for advanced CMOS logic products in particular, has been a paradigm shift in wiring materials, reliability physics, and architecture – the latter by both dual damascene and hierarchical scaling. The net result has been the ability to circumvent, to a significant degree, the “RC crisis” which arises in CMOS wiring as a result of dimensional scaling.

Today, our BEOL work has begun for the 22 nm CMOS node, which represents our 8th Cu generation, and a 1/10x scaling from the original Cu interconnects introduced. By and large, the same integration scheme, materials, and processes have successfully persisted, with only incremental changes for continuous improvements. Some of these will be discussed. This success and longevity are attributed to optimal initial choices, and a focus on reliability, manufacturability, and performance at each node, with only incremental changes.

We have qualified our 6th major CMOS node (45 nm) for manufacturing with the lowest dielectric constant wiring levels using k=2.4 porous SiCOH. The general roadmap for BEOL and FEOL are shown in Fig. 1, spanning 10 years back and several years to the future. Incremental reductions in silicate glass dielectric constant by doping and porosity have been accomplished. This has gone from k=4.1 (undoped silicate glass) to k=3.6 by fluorine doping (0.18 μm generation), to k=3.0 by carbon doping (methyl groups) in 90 nm, to increased carbon doping for k=2.7 in 65 nm, by increased porosity to reduce density for k=2.4, and in development, the added formation of vacuum gaps (“air gaps”) with k=1.0. The “effective” dielectric constants seen by the multilevel wiring environment are higher than these k numbers, due to inclusion of the higher-k thin barrier cap layer of SiNx (k=7.0) or SiCNH (k~5.0 and extending lower). The effective dielectric constants corresponding the the above list of insulators are 4.3, 3.8, 3.2, 2.9, 2.7, and 2.0, respectively. Decreasing the dielectric constant of silicate glasses comes with a concomitant decrease in film cohesive strength, whereas our airgap scheme does not compromise overall chip mechanical properties significantly below that of the native dielectrics.

Consideration of the known prospects for conductors and insulators suggests Cu with (organo-) silicate glass will continue as the predominant scheme. Global (non-length scaled) wiring performance will start to degrade drastically, however, as we migrate from the 90 nm to the 22 nm node, as depicted by the upper bars in Fig. 2. Some of this degradation is mitigated by incremental innovations such as viable lower-k and ultralow-k SiCOH insulators and taller Cu wire aspect ratios, as shown by the middle bars. However, the general trend is still dire. Implementation of directed air gaps (right bars) reduces nested wiring capacitances by ~35% and helps

significantly to flatten the trend, although by 22 nm there is still incomplete relief.

In order to succeed with ever-weaker insulators, we have built on there has been a successive learning and engineering improvements to strengthen the relevant insulators, film mechanical properties, and chip-package mechanical properties. This topical area has been an essential enabler to modern manufacturable Cu/low-k CMOS chips, and will be discussed in further detail.

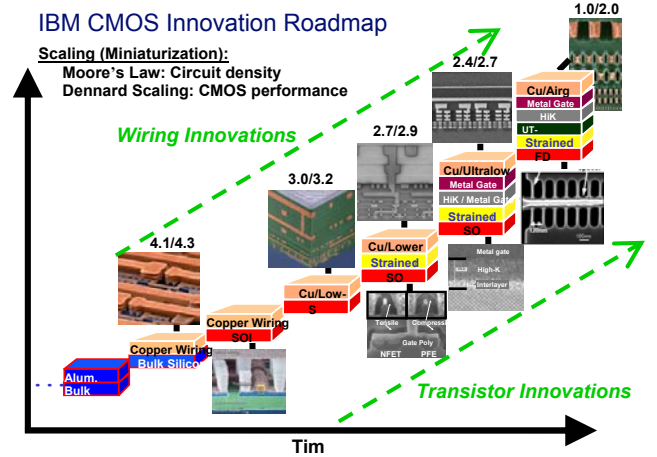


Fig 1 : Ten years of “Scaling by Innovation” to retain upward CMOS performance trend.

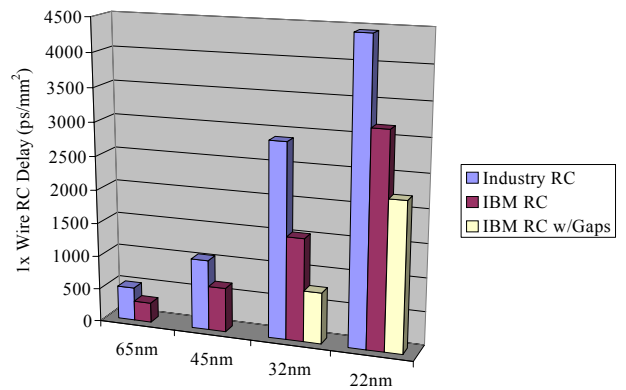


Fig 2 : Trends for global 1x RC wire delay vs. CMOS node.

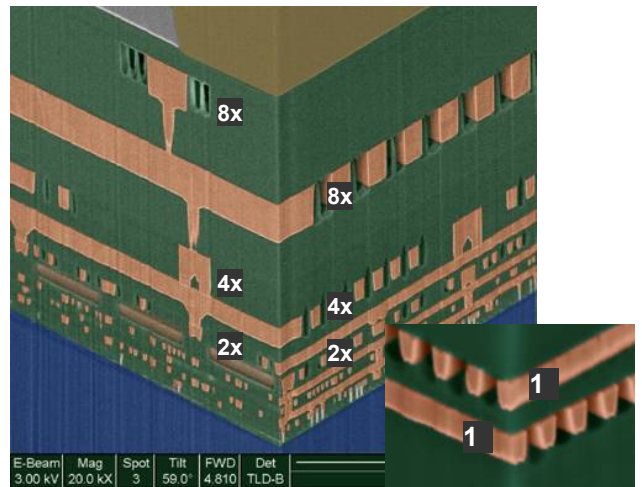


Fig 3 : Airgap BEOL on 65 nm microprocessor.